AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference from a first pair of potential lines; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of potentials having a relatively large potential difference from a second pair of potential lines,

wherein a substrate ~~potentials~~ potential of MIS transistors ~~are~~ is commonly used by said first and second logic gates, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of

potential lines, and further have a portion of at least one substrate potential line which supplies said substrate potential.

2. (Previously Presented) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a substrate potential, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

3. (Previously Presented) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by the respective substrate potentials.

4. (Previously Presented) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a substrate potential, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

5. (Previously Presented) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials.

6. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference from a first pair of potential lines; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of potentials having a relatively large potential difference

from a second pair of potential lines,

wherein said first and second logic gates have MIS transistors, and a well region in which an MIS transistor of said first logic gate is formed and a well region in which an MIS transistor of said second logic gate is formed are made common for each conduction type, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies a substrate potential to said well regions.

7. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference from a first pair of potential lines; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of potentials having a relatively large potential difference

from a second pair of potential lines,

wherein said first and second logic gates have MIS transistors, and a well region in which an MIS transistor of said first logic gate is formed and a well region in which an MIS transistor of said second logic gate is formed are electrically connected for each conduction type, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies a substrate potential to said well regions.

8. (Previously Presented) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in the well region thereof, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

9. (Previously Presented) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective potentials of the well regions thereof, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by respective potentials of the well regions thereof.

10. (Previously Presented) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of the well region thereof, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

11. (Previously Presented) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel

type MIS transistor to which substrate biases are applied in a reverse direction by respective potentials in the well regions thereof.

12. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source in an active operation mode, a first pair of a high potential and a low potential from a first pair of potential lines; and

a second logic gate using, as an operation power source in said active operation mode, a second pair of a high potential and a low potential having a potential difference larger than that of said first potential pair from a second pair of potential lines,

wherein a substrate potential of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other, and

at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and

wh rein said first logic gate and said second logic gate each have two pairs of potential line portions,

respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies said substrate potential.

13. (Previously Presented) A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than said first high potential and a second low potential lower than said first low potential, and said substrate potential is one of a high potential side substrate potential between said first and second high potentials and a low potential side substrate potential between said first and second low potentials.

14. (Original) A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than the first high potential and a second low potential lower than said first low potential, said second

high potential is used as a high potential side substrate potential, and said second low potential is used as a low potential side substrate potential.

15. (Original) A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than the first high potential and said low potential, a potential between said first and second high potentials is used as a high potential side substrate potential, and potential higher than said first low potential is used as a low potential side substrate potential.

16. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate connected to a first pair of a high potential line and a low potential line in an active operation mode; and

a second logic gate connected to a second pair of a high potential line and a low potential line in said active operation mode, said second ~~line~~ pair of potential lines

having a potential difference larger than that of said first pair of potential ~~line pair~~lines,

wherein a substrate potential line is commonly used for supplying a substrate potential to an MIS transistor of said first logic gate and for supplying a substrate potential to an MIS transistor of said second logic gate, ~~and~~

wherein at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies said substrate potential.

17. (Currently Amended) A semiconductor integrated circuit according to claim 16, wherein

said first ~~potential line~~ pair of potential lines includes a first high potential line and a first low potential line,

said second ~~potential line~~ pair of potential lines includes a second high potential line having a potential higher than that of said first high potential line and a second low potential line having a potential lower than said first low potential line, and

said substrate potential line is one of a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of said second high potential line, and a low potential side substrate potential line having a potential between the potential of said first low potential line and the potential of said second low potential line.

18. (Original) A semiconductor integrated circuit according to claim 16, wherein said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair includes a second high potential line having a potential higher than that of the first high potential line and a second low potential line having a potential lower than that of said first low potential, and

said second high potential line is used as a high potential side substrate potential line, and said second low potential line is used as a low potential side substrate potential line.

19. (Amended) A semiconductor integrated circuit according to claim 16, wherein said first ~~potential line~~ pair of potential lines includes a first high potential line and a first low potential line,

said second ~~potential line~~ pair of potential lines includes said first low potential line and a second high potential line having a potential higher than that of the first high potential line, and

said substrate potential line is one of a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of the second high potential line, and a low potential side substrate potential line having a potential higher than the potential of said first low potential line.

20. (Currently Amended) A semiconductor integrated circuit having a circuit region in which a number of logic gates each having an MIS transistor are arranged on a

semiconductor substrate,

wherein said circuit region has a well region including portions shared by a substrate potential for each conduction type of MIS transistor,

a first logic gate using, as an operation power source in an active operation mode, a first pair of potentials having a relatively small potential difference from a first pair of potential lines and a second logic gate using, as an operation power source in said active operation mode, a second pair of potentials having a relatively large potential difference from a second pair of potential lines are formed in said well region,

in said well region, a p-type well portion in which an n-channel type MIS transistor is formed and an n-type well portion in which a p-channel type MIS transistor is formed are adjacent to each other, ~~and~~

metal lines for supplying said first pair of potentials, said second pair of potentials, and a substrate ~~potentials~~ potential are arranged on said well region, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of

potential lines, and further have a portion of at least one substrate potential line which supplies said substrate potential.

21. (Previously Presented) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a substrate potential, and

said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

22. (Previously Presented) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials, and

said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by the respective substrate potentials.

23. (Previously Presented) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor to which substrate bias is applied in a reverse direction by a substrate potential, and

said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

24. (Previously Presented) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials.

Claims 25-36 (Cancelled)

37. (Currently Amended) A design data recording medium on which design data for forming an integrated circuit on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first mask pattern data for determining a figure pattern for forming a well region on which a plurality of logic gates is formed;

second mask pattern data for determining a figure pattern for forming a first ~~line~~ pair of potential lines, a second ~~line~~ pair of potential lines and a third ~~line~~ pair of potential lines on said well region; and

third mask pattern data for determining a figure pattern for forming a plurality of connectors,

wherein a first group of said connectors connects said first ~~line~~ pair of potential lines and portions of said well region,

wherein a second group of said connectors connects said second ~~line~~ pair of potential lines and a first group of said logic gates for supplying a first potential difference to said first group of logic gates in an active operation mode, ~~and~~

wherein a third group of said connectors connects said third ~~line~~ pair of potential lines and a second group of said logic gates for supplying a second potential difference which is larger than said first potential difference to said second group of logic gates in said active operation mode, and

wherein said second mask pattern includes a figure pattern for forming said first line pair and said second line pair in parallel in one row pattern.

38. (Currently Amendment) A design data recording medium on which design data for designing an integrated circuit to be formed on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first function description data for determining a function of a first logic gate to which an operation power source is supplied, in an active operation mode, from a first pair of potential lines having a relatively small potential difference and a substrate potential is supplied from a substrate potential line; and

second function description data for determining a function of a second logic gate to which an operation power source is supplied, in said active operation mode, from a second pair of potential lines having a relatively large potential difference and a substrate potential is supplied from a substrate potential line connected to said substrate potential line,

wherein descriptions for the first logic gate and the second logic gate have description of said first line pair and said second line pair in common.

39. (Previously Presented) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in the well region thereof, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

40. (Previously Presented) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective potentials of the well regions thereof, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by respective potentials of the well regions thereof.

41. (Previously Presented) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of the well region thereof, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

42. (Previously Presented) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective potentials in the well regions thereof.

43. (Previously Presented) A semiconductor integrated circuit according to claim 1, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

44. (Previously Presented) A semiconductor integrated circuit according to claim 6, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

45. (Previously Presented) A semiconductor integrated circuit according to claim 7, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

46. (Previously Presented) A semiconductor integrated circuit according to claim 12, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

47. (Currently Amended) A semiconductor integrated circuit according to claim 16, wherein said first and second logic gates are connected to said first and second

~~potential line~~ pairs of potential lines, respectively, in a standby mode.

48. (Previously Presented) A semiconductor integrated circuit according to claim 20, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

49. (Currently Amended) A semiconductor integrated circuit according to claim 37, wherein said first and second groups of logic gates are supplied from said second and third ~~line~~ pairs of potential lines, respectively, in a standby mode.

50. (Currently Amended) A semiconductor integrated circuit according to claim 38, wherein said first and second logic gates are supplied from said first and second potential ~~line~~ pairs of potential lines, respectively, in a standby mode.

51. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate which is supplied with a first potential difference as a sole operation power source from a first ~~line~~ pair of potential lines; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second ~~line~~ pair of potential lines,

wherein said first potential difference is smaller than said second potential difference, ~~and~~

wherein a substrate potential of MIS transistors is commonly used by said first and second logic gates, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies said substrate potential.

52. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate which is supplied with a first potential difference as a sole operation power source from a first ~~line~~ pair of potential lines; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second ~~line~~ pair of potential lines,

wherein said first potential difference is smaller than said second potential difference, ~~and~~

wherein said first and second logic gates have MIS transistors, and a well region in which an MIS transistor of said first logic gate is formed and a well region in which an MIS transistor of said second logic gate is formed are made common for each conduction type, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies a substrate potential to said well regions.

53. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate which is supplied with a first potential difference as a sole operation power source from a first ~~line~~ pair of potential lines; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second ~~line~~ pair of potential lines,

wherein said first potential difference is smaller than said second potential difference, ~~and~~

wherein said first and second logic gates have MIS transistors, and a well region in which an MIS transistor of said first logic gate is formed and a well region in which an MIS transistor of said second logic gate is formed are electrically connected for each conduction type, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies a substrate potential to said well regions.

54. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate which is supplied with a first potential difference as a sole operation power source from a first ~~line~~ pair of potential lines of a high potential

and a low potential; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second ~~line~~ pair of potential lines of a high potential and a low potential,

wherein said first potential difference is smaller than said second potential difference,

wherein a substrate potential of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other, ~~and~~

wherein at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies said substrate potential.

55. (Currently Amended) A semiconductor integrated circuit comprising:

a first logic gate connected to receive a first potential difference as a sole operation power source from a first pair of potential lines of a high potential ~~line~~ and a low potential ~~line~~; and

a second logic gate connected to receive a second potential difference as a sole operation power source from a second pair of potential lines of a high potential ~~line~~ and a low potential ~~line~~,

wherein said first potential difference is smaller than said second potential difference,

wherein a substrate potential line is commonly used for supplying a substrate potential to an MIS transistor of said first logic gate and for supplying a substrate potential to an MIS transistor of said second logic gate, ~~and~~

wherein at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one

substrate potential line which supplies said substrate potential.

56. (Currently Amended) A semiconductor integrated circuit having a circuit region in which a number of logic gates each having an MIS transistor are arranged on a semiconductor substrate,

wherein said circuit region has a well region including portions shared by a substrate potential for each conduction type of MIS transistor,

a first logic gate is supplied with a first potential difference as a sole operation power source from a first ~~line~~ pair of potential lines,

a second logic gate is supplied with a second potential difference as a sole operation power source from a second ~~line~~ pair of potential lines,

said first logic gate and said second logic gate are formed in said well region,

said first potential difference is smaller than said second,

in said well region, a p-type well portion in which an n-channel type MIS transistor is formed and an n-type well portion in which a p-channel type MIS transistor is formed

are adjacent to each other, ~~and~~

metal lines for supplying said first potential difference, said second potential difference, and a substrate potential are arranged on said well region, and

wherein said first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of said first pair of potential lines and portions of said second pair of potential lines, and further have a portion of at least one substrate potential line which supplies said substrate potential.

57. (Currently Amended) A design data recording medium on which design data for forming an integrated circuit on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first mask pattern data for determining a figure pattern for forming a well region on which a plurality of logic gates is formed,

second mask pattern data for determining a figure pattern for forming a first ~~line~~ pair of potential lines, a second ~~line~~ pair of potential lines and a third ~~line~~ pair of potential lines on said well region, and

third mask pattern data for determining a figure pattern for forming a plurality of connectors,

wherein a first group of said connectors connects said first ~~line~~ pair of potential lines and portions of said well region,

wherein a second group of said connectors connects said second ~~line~~ pair of potential lines and a first group of said logic gates for supplying said first group of logic gates with a first potential difference as a sole operation power source from said second ~~line~~ pair of potential lines, and

wherein a third group of said connectors connects said third ~~line~~ pair of potential lines and a second group of said logic gates for supplying said second group of logic gates with a second potential difference, which is larger than said first potential difference, as a sole operation power source from said third ~~line~~ pair of potential lines, and

wherein said second mask pattern includes a figure pattern for forming said first pair of potential lines and said second pair of potential lines in parallel in one row pattern.

58. (Currently Amended) A design data recording medium on which design data for designing an integrated circuit to be formed on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first function description data for determining a function of a first logic gate which is supplied with a first potential difference as a sole operation power source from a first pair of potential lines and a substrate potential from a substrate potential line;

second function description data for determining a function of a second logic gate which is supplied with a second potential difference as a sole operation power source from a second pair of potential lines and a substrate potential from said substrate potential line; and

third function description data for determining said first potential difference to be smaller than said second potential difference,

wherein the description of the first logic gate and the description of the second logic gate have the first pair of potential lines and the second pair of potential lines in common.

59. (Previously Presented) A design data recording medium according to claim 37,

wherein said well region includes a first well portion and a second well portion,

wherein said first mask pattern data includes fourth mask pattern data and fifth mask pattern data,

wherein said fourth mask pattern data is for determining a figure pattern for forming the first well portion, and

wherein said fifth mask pattern data is for determining a figure pattern for forming the second well portion.

Claims 60-61 (Cancelled)